**LISTING OF THE CLAIMS:**

Claim 1 (Cancelled).

2. (Currently Amended) A power saving cache comprising:

circuitry to dynamically reduce the logical size of the cache in order to save power by powering off selected areas of the cache; ~~and~~

means for determining an optimal cache size for balancing power and performance; and

means for maintaining coherency of data in the cache, as the size of the cache is altered, by ensuring that copies of all data elements in the cache exist in an area of the cache not powered off.

3. (Original) A power saving cache according to Claim 2, wherein the means for determining an optimal cache size includes hardware means.

4. (Original) A power saving cache according to Claim 2, wherein the means for determining an optimal cache size includes software means.

Claim 5 (Cancelled).

6. (Currently Amended) A power saving cache according to Claim ~~5~~ 2, wherein some of the data in the cache is modified data, and the means for maintaining coherency includes means for handling said modified data.

7. (Previously Presented) A power saving cache according to Claim 2, wherein the circuitry includes means for partitioning the cache in one of several ways to provide a desired configuration and granularity.

Claim 8 (Cancelled).

9. (Previously Presented) A power saving cache according to Claim 2, wherein the cache is a set associative cache with N-ways, and the circuitry includes means to partition the cache along said ways.

10. (Currently Amended) A method of operating a power saving cache comprising:

using circuitry to dynamically reduce the logical size of the cache in order to save power by powering off selected areas of the cache; ~~and~~

determining an optimum size for the cache for balancing power and performance given a set of power and performance criteria; and

maintaining coherency of data in the cache, as the size of the cache is altered, by ensuring that copies of all data elements in the cache exist in an area of the cache not powered off.

11. (Original) A method according to Claim 10, wherein the cache is a set associative cache including N-ways, and the step of using circuitry to dynamically reduce the logical size of the cache includes the step of using the circuitry to partition the cache along the ways.

12. (Original) A method according to Claim 11, wherein each of said N ways is individually powered.

Claims 13 and 14 (Cancelled).

15. (Currently Amended) A method according to Claim ~~14~~ 12, wherein some of the data in the cache is modified data, and the step of maintaining integrity of the data includes the step of, before powering off one of the sections of the cache, saving any modified data in said one section of the cache.

16. (Currently Amended) A method of operating a power saving cache, wherein the cache includes data and some of the data in the cache is modified data, the method comprising:

using circuitry to dynamically reduce the logical size of the cache in order to save power;

maintaining integrity of the data as the size of the cache is altered;

powering off sections of the cache;

wherein the step of maintaining integrity of the data includes the step of, before powering off one of the sections of the cache, saving any modified data in said one section of the cache and ensuring that copies of all data elements in the cache exist in sections of the cache not powered off; and

further comprising the step of determining an optimum size for the cache given a set of power and performance criteria, and wherein the step of using circuitry includes the step of using circuitry to reduce the size of the cache to said optimum size.

17. (Original) A method according to Claim 16, wherein the step of determining an optimum size includes the step of using one of a predefined set of hardware techniques to determine said optimum size.

18. (Original) A method according to Claim 16, wherein the cache is used in a processor, and the method includes the further steps of:

running on the processor a cache size adjustment routine; and

feeding information to said routine to determine the optimum size of the cache.

19. (Currently Amended) A method of operating a power saving cache comprising:

using circuitry to dynamically reduce the logical size of the cache in order to save power by powering off selected areas of the cache; and

maintaining coherency of data in the cache, as the size of the cache is altered, by ensuring that copies of all data elements in the cache exist in an area of the cache not powered off;

wherein the using step includes the step of partitioning the cache in one of a given number of ways to provide a desired configuration and granularity, said given number of ways comprising (i) equal sized partitions, and (ii) binary weighted with or without a constantly powered way.

20. (New) A method according to Claim 10, wherein the cache includes a multitude of cache entries and each of said entries is identified by an associated tag, and the step of maintaining coherency of data in the cache includes the step of:

when the size of the cache is altered, purging the entire contents of the cache to reorder the cache, and adding a bit value to each tag.